Docket No.: 3449-0413PUS1 Page 6 of 17

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AMENDMENTS TO THE CLAIMS

1. (Original) A nitride semiconductor LED, comprising:

a substrate;

a GaN-based buffer layer formed on the substrate;

Al_vGa_{1-v}N/GaN short period superlattice (SPS) layers formed on the GaN-based buffer

layer in a sandwich structure of upper and lower layers having an undoped GaN layer or an

indium-doped GaN layer interposed therebetween (where, $0 \le y \le 1$) (where $0 < y \le 1$);

a first electrode layer of an n-GaN layer formed on the upper Al_vGa_{1-v}N/GaN SPS layer;

an active layer formed on the first electrode layer; and

a second electrode layer of a p-GaN layer formed on the active layer.

2. (Currently Amended) The nitride semiconductor LED of claim 1, wherein the GaN-

based buffer layer has a triple-structured AlvInxGal-xvN/InxGal-xN/GaN AlvInxGal-(x+y)N/InxGal-

_xN/GaN laminated (Here, where $0 \le x \le 1$, $0 \le y \le 1$), a double-structured In_xGa_{1-x}N/GaN

laminated (Here, where $0 \le x \le 1$), or a super-lattice-structured (SLS) $In_xGa_{1-x}N/GaN$ laminated

(Here, where $0 \le x \le 1$).

3. (Original) The nitride semiconductor LED of claim 1, further comprising the

undoped GaN layer or the indium-doped GaN layer on the GaN-based buffer layer.

4. (Currently Amended) A nitride semiconductor LED, comprising:

JTE/REG/ei

Docket No.: 3449-0413PUS1 Application No. 10/517,818 Amendment dated September 11, 2006

Reply to Office Action of May 9, 2006

a substrate;

a GaN-based buffer layer formed on the substrate;

an undoped GaN layer or an indium-doped GaN layer formed on the GaN-based buffer

layer;

Al_vGa_{1-v}N/GaN short period superlattice (SPS) layers formed on the undoped GaN layer

or the indium-doped GaN layer, in a sandwich structure of upper and lower layers having the

undoped GaN layer or the indium-doped GaN layer interposed therebetween (Here, $0 \le y \le 1$)

(where $0 < y \le 1$);

a first electrode layer of an n⁺-GaN layer formed on the upper Al_vGa_{1-v}N/GaN SPS layer

and containing a high concentration of dopants;

an n-GaN layer formed on the first electrode layer and containing a low concentration of

dopants;

an active layer formed on the n-GaN layer; and

a second electrode layer of a p-GaN layer formed on the active layer.

The nitride semiconductor LED of claim 4, wherein the 5. (Currently Amended)

GaN-based buffer layer has triple-structured Al_vIn_xGa_{1-x5v}N/In_xGa_{1-x}N/GaN

 $Al_vIn_xGa_{1-(x+v)}N/In_xGa_{1-x}N/GaN$ laminated (Here, where $0 \le x \le 1$, $0 \le y \le 1$), a double-structured

 $In_xGa_{1-x}N/GaN$ laminated (Here, where $0 \le x \le 1$), or a super-lattice-structured (SLS)

 $In_xGa_{1-x}N/GaN$ laminated (Here, where $0 \le x \le 1$).

JTE/REG/ej

Page 7 of 17

Amendment dated September 11, 2006 Reply to Office Action of May 9, 2006

6. (Original) A nitride semiconductor LED, comprising:

a substrate;

a GaN-based buffer layer formed on the substrate;

a first electrode layer of an n+-GaN layer formed on the GaN-based buffer layer and

containing a high concentration of dopants;

an n-GaN layer formed on the first electrode layer and containing a low concentration of

dopants;

an active layer formed on the n-GaN layer; and

a second electrode layer of a p-GaN layer formed on the active layer.

7. (Original) The nitride semiconductor LED of claim 6, wherein the dopant

concentration of the n⁺-GaN layer is more than 1x10¹⁸/cm³.

8. (Original) The nitride semiconductor LED of claim 6, wherein the dopant

concentration of the n-GaN layer is less than 1x10¹⁸/cm³.

9. (Original) The nitride semiconductor LED of claim 6, wherein the dopant

concentration of the n-GaN layer is $1 \times 10^{17} / \text{cm}^3$.

10. (Currently Amended) The nitride semiconductor LED of claim 6, wherein the GaN-

based buffer layer has a triple-structured AlyInxGa1-x5yN/InxGa1-xN/GaN AlyInxGa1-(x+y)N/InxGa1-

_xN/GaN laminated (Here, where $0 \le x \le 1$, $0 \le y \le 1$), a double-structured In_xGa_{1-x}N/GaN

JTE/REG/ej

Reply to Office Action of May 9, 2006

laminated (Here, where, $0 \le x \le 1$), or a super-lattice-structured (SLS) $In_xGa_{1-x}N/GaN$ laminated

(Here, where $0 \le x \le 1$).

11. (Currently Amended) The nitride semiconductor LED of claim 6, further

comprising Al_vGa_{1-v}N/GaN short period superlattice (SPS) layers formed on the GaN-based

buffer layer in a sandwich structure of upper and lower parts having an undoped GaN layer or an

indium-doped GaN layer interposed therebetween (Here, $0 \le y \le 1$) (where $0 < y \le 1$).

12. (Currently Amended) A fabrication method of a nitride semiconductor LED, the

method comprising the steps of:

growing-up a GaN-based buffer layer on a substrate;

forming Al_vGa_{1-v}N/GaN short period superlattice (SPS) layers on the GaN-based buffer

layer in a sandwich structure of upper and lower parts having an undoped GaN layer or an

indium-doped GaN layer interposed therebetween (Here, $0 \le y \le 1$);

forming a first electrode layer of an n⁺-GaN layer containing a high concentration of

dopants, on the upper Al_vGa_{1-v}N/GaN SPS layer;

forming an active layer on the first electrode layer; and

forming a second electrode layer of [[an]] a p-GaN layer on the active layer.

13. (Original) The fabrication method of claim 12, further comprising the step of

forming an n-GaN layer containing a low concentration of dopants, between the first electrode

layer of the n⁺-GaN layer and the active layer.

JTE/REG/ej

Docket No.: 3449-0413PUS1

Page 9 of 17

Application No. 10/517,818 Amendment dated September 11, 2006

Reply to Office Action of May 9, 2006

Docket No.: 3449-0413PUS1

Page 10 of 17

14. (Original) The fabrication method of claim 12, wherein the GaN-based buffer layer

is, using a MOCVD equipment, grown-up to have a 50-800 Å thickness at a 500-800 °C

temperature and in an atmosphere having H2 and N2 carrier gases supplied while having TMGa,

TMIn, TMAl source gas introduced and simultaneously having NH₃ gas introduced.

15. (Original) The fabrication method of claim 12, wherein the GaN-based buffer layer is

grown-up with a 5-300µmol/min flow rate of the TMGa, TMIn, TMAl source gas and a 100-700

torr growth pressure.

16. (Currently Amended) The fabrication method of claim 12, wherein the GaN-based

buffer layer has a triple-structured AlvInxGal-xivN/InxGal-xN/GaN AlvInxGal-(x+y)N/InxGal-

_xN/GaN laminated (Here, where $0 \le x \le 1$, $0 \le y \le 1$), a double-structured In_xGa_{1-x}N/GaN

laminated (Here, where $0 \le x \le 1$), or a super-lattice-structured (SLS) In_xGa_{1-x}N/GaN laminated

(Here, where $0 \le x \le 1$).

17. (Original) The fabrication method of claim 12, further comprising the step of

forming an undoped GaN layer or an indium-doped GaN layer on the GaN-based buffer layer.

18. (Original) The fabrication method of claim 12, wherein the dopant concentration of

the n^+ -GaN layer is more than $1x10^{18}$ /cm³.

JTE/REG/ei

Application No. 10/517,818 Amendment dated September 11, 2006 Reply to Office Action of May 9, 2006 Docket No.: 3449-0413PUS1

Page 11 of 17

19. (Original) The fabrication method of claim 13, wherein the dopant concentration of the n-GaN layer is 1×10^{17} /cm³.

20. (Original) The fabrication method of claim 13, wherein the n-GaN layer is formed with a semi-insulating layer.